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Atty. Docket No. OPP031047US

IN THE UNITED STATES PATENT & TRADEMARK OFFICE

IN RE APPLICATION OF:	:
Jae-Won HAN	: GROUP ART UNIT: 2812
APPLICATION NO: 10/751,172	:
FILED: DECEMBER 30, 2003	: EXAMINER: NGUYEN, Ha T.

FOR: METHOD FOR MANUFACTURING SILICIDE AND SEMICONDUCTOR WITH THE SILICIDE

I hereby certify that this document is being facsimile transmitted to the USPTO or deposited with the United States Postal Service as first class mail in an envelope addressed to Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on March 15, 2006.

By: _____
~~Jennie Heston~~ Andrew Fortney
Reg. No. 34,606

DECLARATION UNDER 37 C.F.R. 1.132

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SIR:

Now comes Jae-Won HAN, who declares and states that:

1. I am an electrical engineer, currently employed by DongbuAnam Semiconductor, Inc., in the Advanced Nano-technology Development group. I have been continuously employed by DongbuAnam Semiconductor, Inc. since 1996. Prior to 2006, I was employed by Dr. KH Kim, where my duties included research and development work in the area of BEOL process.

2. I received a Bachelor's degree in Physics from Sung-Kyun-Kwan University in 1997, a Master's degree in Applied Physics from Sung-Kyun-Kwan University in 1992, and a Ph.D. in Applied Physics from Sung-Kyun-Kwan University in 1997.

3. I have read the above-identified application and am familiar with the subject matter disclosed and claimed therein. I am also familiar with metal silicides and salicides, structures in semiconductor devices containing the same, and techniques used in the art of semiconductor manufacturing for making such structures.

4. I understand that one of the independent claim(s) of the above-identified application is directed to a method of manufacturing silicide, comprising the steps of:

a) cleaning a semiconductor substrate with a transistor formed thereon, the transistor including a source electrode, a drain electrode and a gate electrode;

b) placing the cleaned semiconductor substrate into a sputter chamber in a deposition equipment, and heating the semiconductor substrate to a temperature of from greater than 450 to 600°C;

c) initially forming a monosilicide at the same time of as depositing a metal film under a state where the semiconductor substrate is heated at a the temperature of from greater than 450 to 600°C;

d) removing residual metal film not used for the formation of silicide; and

e) annealing the semiconductor substrate.

5. The following experiments were performed by me or under my supervision and control:

Productivity (Salicide Module Processing)

The processes outlined in the table below were performed on 24 substantially identical silicon wafers (i.e., one lot) to determine the processing time savings provided by the present

invention, as compared to a conventional process reasonably close to the present invention ("Prior Art").

	Steps	Sequence	Process time
Prior art	8	• SC1 Cleaning • HF Cleaning • Plasma Sputter Etch (AMAT Endura PCII Chamber) • Co Sputter Deposition (Applied Materials Endura Co Deposition Chamber, 2kW DC power, 200°C) • Cap/Barrier Layer Sputter Deposition (AMAT Endura TiN Deposition Chamber) • Silicide Formation (RTP Equipment, 500°C, 30 sec) • Free Co Metal Strip • Silicide Anneal (RTP Equipment, 870°C, 30 sec)	6 hrs
The Present Invention	6	• SC1 Cleaning (Cleaning Equipment) • HF Cleaning (Cleaning Equipment) • Plasma Sputter Etch (APPLIED MATERIALS Endura PCII Chamber) • Co Sputter Deposition (APPLIED MATERIALS Endura Co Deposition Chamber : 8kW DC power, 500°C) • Free Co Metal Strip (Wet Equipment) • Silicide Anneal (RTP Equipment, 870°C, 30sec)	4 hrs

6. Except for the Co sputter deposition step and the existence (or lack of) cap metal sputter deposition and silicide formation steps, processing conditions for the processes representative of conventional technology for forming a silicide ("Prior Art" in the above table)

and the present invention were substantially the same. In the process representative of conventional technology, forming a TiN cap/barrier layer was necessary because the wafers had to be transferred to a Rapid Thermal Processing (RTP) chamber for silicide formation.

7. As shown in the above table, the present invention enables reducing the number of steps in the silicide formation process by 25% and the amount of time by 33%, both somewhat surprising results given the reasonable expectation that the invention would enable reduction of only one step in the conventional process (silicide formation).

8. Another unexpected result from the present invention is that the present invention enables use of the RTP equipment for other processing (such as implant diffusion and activation) that would otherwise be used for silicide formation. This unexpected benefit is commercially very important when a semiconductor wafer fabrication facility (commonly referred to as a "Fab") is capacity-constrained, because it enables other wafers to be processed more quickly as well.

9. I understand that another the independent claim(s) of the above-identified application is directed to a method of manufacturing silicide, comprising the steps of:

a) cleaning a semiconductor substrate with a transistor thereon, the transistor including a source electrode, a drain electrode and a gate electrode;

b) placing the cleaned semiconductor substrate into a sputter chamber and sputtering a metal film at a DC power of 2 – 10kW, while heating the semiconductor substrate at a temperature of 450 to 600°C to form silicide;

c) removing residual metal film; and

d) annealing the semiconductor substrate.

10. The following experiment(s) were performed by me or under my supervision and control:

Power vs. Silicide Resistance.

Two experiments were performed to form a metal silicide film, using the same processing equipment and the same recipe, except for the DC power. An Endura metal sputtering machine (from Applied Materials, Santa Clara, California) was used. Sputtering conditions included a wafer temperature of 200°C, using a Ti metal target, a DC power of 2kW or 8kW (note that the deposition times were different at 2 kW vs. 8 kW to form a Ti silicide film of substantially the same thickness), and a pressure of ~0.2 mTorr. A Ti thin film having a thickness of 480 Å was deposited on the metal silicide film. The substrate wafers (a bare Si wafer) was prepared identically, by cleaning with SC1 and HF, using conventional cleaning conditions. The results were as follows:

Sputtering Power	Silicide Resistance
2 kW	2.1 ohm/sq
8 kW	1.8 ohm/sq

11. Based on my experience in the field of semiconductor devices and manufacturing, it is my opinion that a manufacturing process that forms a metal silicide at less than 2 kW would likely not have a sufficiently low resistance to be commercially valuable. In other words, while such silicides could be expected to provide functional integrated circuits, such integrated circuits would be expected to have sufficiently high contact resistance (where the contact includes the metal silicide) to prevent the integrated circuit from exhibiting or achieving a commercially valuable signal processing speed (sometimes known as a "bin," which is frequently characterized by the length of time that a signal travels from input pin to output pin on the integrated circuit).

12. Further, Declarant sayeth not.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are

punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the above-identified application or any patent issued thereon or therefrom.

Jae-Won HAN

03/02/06
Date